EFFICIENT MEASURING OF COMPLEX PROGRAMMABLE LOGIC DEVICE (CPLD) IMPLEMENTED ANALOG-TO-DIGITAL CONVERTERS STATIC PARAMETERS

Sergejs Šarkovskis[1], Sergejs Horošilovs[2]

[1]Transport and Telecommunication Institute
The Faculty of Computer Science and Telecommunication
Lomonosova str. 1/4, LV-1019, Riga, Latvia
E-mail: sergejs.sarkovskis@gmail.com
[2]ALFA RPAP AS
Ropazu str. 140, LV-1006, Riga, Latvia
E-mail: sergejs.sarkovskis@gmail.com

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The precision of analog-to-digital signal conversion plays an important role in digital communication systems. At the present moment, the histogram method is the method mainly used for measuring analog-to-digital converter (ADC) static parameters (Kester, 2005), such as differential nonlinearity (DNL) and integral nonlinearity (INL). In such case the ADC input signal is being changed linearly and output data is used to construct a histogram (Blair, 1994), thus calculating the number of specific codes occurrences. The main problem of such method implementation is necessity to store a large volume of data – ADC output code words during the collection of information. It is usual to use memory modules for such purpose. This article focuses on implementation of histogram method of ADC static parameters measuring based on inexpensive complex programmable logic device (CPLD) arrays. The article proposes histogram real-time calculation algorithm for array, which allows reducing volume of required memory or stopping using it entirely.

References

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