done by short circuiting both prototypes and measuring the impedance at SMA port. The measurements have been done using vector network analyzer (VNA) Rohde&Schwarz ZVRE.

Measurement and modeling results are compared in Fig.3. Measurement results below 100kHz are noisy doe to the fact that low impedance is measured and measurement method that uses VNA do not have the highest accuracy when very low impedances are measured. It can be concluded that 3D models of both prototypes are well built as modeling and measurement results fit quite well. The measured impedance has inductive characteristic. It is obvious, as the short circuited PCB's creates loops. Prototype PCB1 impedance is lower than PCB2 impedance, due to the fact that it has tracks with a higher cross section area and tracks are creating loop with a smaller area. Higher track cross section area and smaller loop area should lead also to lower impedance when capacitors will be mounted on PCB's.

III. CAPACITOR MODELING

Very accurate modeling of capacitors is difficult task and it takes huge amount of memory and computational power, because internal geometry of film capacitors is very complex. Therefore two simplified capacitor models (Fig.5) have been proposed by T. Oliveira, et.al [6]. The first one (Fig.5(a)) is based on the Dowell approximation [13]. The model can only describe magnetic properties of capacitors and therefore a series capacitance has to be added [6]. In order to reduce computational time and power at the cost of modeling accuracy, a more simplified capacitor model with only one electrode (Fig.5(b)) has been proposed in [6].

Both models (Fig.5) proposed in [6] must be calibrated and the resistive part variables (such as electrode spacing k, thickness t and resistivity ρ) must be calculated.

It is possible to propose much simpler model that eliminates the usage of conductive material and is more suitable for usage with modern 3D electromagnetic modeling software as ANSYS HFFS and CST MWS. In this case the capacitor capacitance C and ESR must be represented by lumped elements. The structure of model is made out of perfect electric conductor. The physical size of models represents exact size of capacitor conductive parts, without outer insulation shell, as in Fig.4(b). There are proposed three models, starting from most complex, that represents the inner structure of capacitor more detailed - Cap1, to the less complex - Cap3, that leads to the lowest memory consumption and computational power (Fig.6).

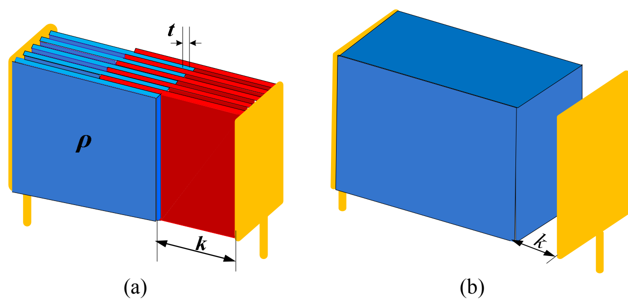

Fig. 5. (a) Capacitor model for 3D electromagnetic modeling [6] and (b) its simplified version proposed in [6].

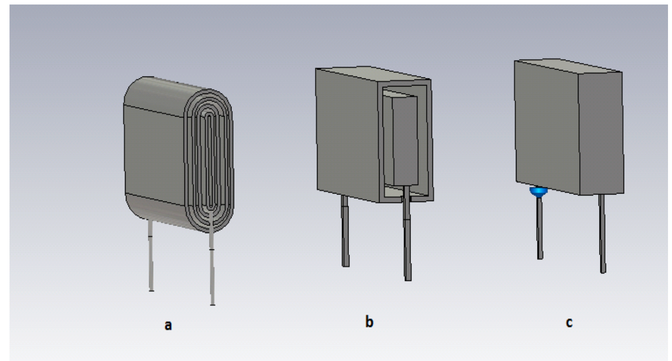

Fig. 6. Capacitor models proposed in the paper: (a) the most complex capacitor model proposed - Cap1; (b) medium complex capacitor model proposed - Cap2; (c) the simplest capacitor model proposed - Cap3.

The first two proposed models - Cap1 and Cap2, in plain manner represents the capacitor metalized film layer structure, to verify the coupling properties to nearby components. The Cap3 model is modeled as rectangle and does not represent inner metalized film layer structure, but only the exact overall dimensions of capacitor conductors. Capacitor models also represent only magnetic behavior of component, thus they are supplemented by capacitance and series resistance using lumped elements. In CST MSW the capacitors can be meshed using tetrahedral and hexahedral mesh. The meshcell number is compared for all capacitor prototypes in Table 1. All the boundary settings, materials and mesh settings are the same for all models. It should be mentioned that no optimization of mesh setting have not been done to evaluate the situation for all models in the same conditions.

TABLE1. MESHCELL COUNT FOR PROPOSED CAPACITOR MODELS

Mesh type	Capacitor model		
	Cap1 Meshcells	**Cap2** Meshcells	**Cap3** Meshcells
Tetrahedral	85.474	25.219	16.878
Hexahedral	47.376	22.644	18.432

The least complex capacitor model - Cap3, has the least complex mesh that leads to the lowest meschell number. Mesh and calculation time can be compared to evaluate all three capacitor models. CST MSW provides wide amount of solvers to use. Time domain and frequency domain solvers have been chosen, to use, for problem solving. Frequency domain solver can be used with tetrahedral and hexahedral mesh, while time domain solver only with hexahedral mesh type. In Table 2, modeling time for three capacitor models is compared for both solvers with different mesh types. For frequency domain only one frequency sample is calculated, while time domain solver calculates all the defined frequency range 100kHz-50MHz, therefore it should be mentioned that in Table 2, capacitor model calculation times are compared, not the solvers itself. Using both solvers and different mesh types it is obvious that Cap3 model calculation takes at least 30% less than Cap2 calculation and at least 250% less time than Cap1 calculation, if frequency domain solver with hexahedral mesh is used. For

time domain solver the difference in calculation time is higher - Cap3 model calculation takes at least 16% less than Cap2 calculation and at least 1280% less time than Cap1 model calculation.

In further sub-clauses the evaluation of all the three models performance are verified and analyzed to prove, that it is possible to model capacitors, used in EMI filters, using 3D electromagnetic modeling software with high accuracy, without describing capacitor with several thousands of metalized film layers.

TABLE2. MESHCELL NUMBER FOR PROPOSED CAPACITOR MODELS

Solver / mesh type	Capacitor model		
	Cap1 h:min	**Cap2** h:min	**Cap3** h:min
Time domain / Hexahedral	14:05	1:11	1:01
Frequency domain / Hexahedral	1:10	0:26	0:20
Frequency domain / Tetrahedral	2:40	0:51	0:32

IV. CAPACITOR MODEL VERIFICATION

The capacitor models for further successful usage were validated. The set of S-parameter and Z-parameter measurements were carried out:

1. One capacitor mounted on PCB (Z_{11} measured);
2. Two capacitors mounted on PCB (Z_{11} measured);
3. Two capacitors mounted on PCB (S-parameters measured);
4. Two capacitors mounted on modified PCB, with one solid and one split track (S- parameters measured).

A. Z_{11} parameter measurements if one capacitor is mounted on PCB

To verify the performance of both - PCB and all proposed capacitor models, measurements were carried out and input impedance at SMA port were measured. The 3D models for PCB1 with mounted capacitors, with tetrahedral mesh view and measured prototype are shown in Fig.7. The measurement and modeling results are compared in Fig.8 and Fig.9 for both PCB1 and PCB2, respectively. In this case impedance Z_{11} characterizes capacitor impedance, PCB layout impedance and

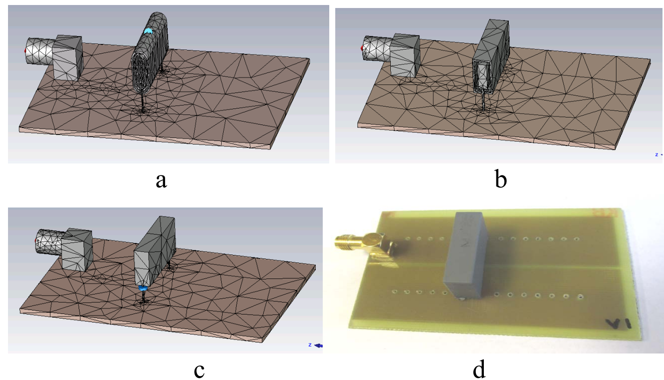

Fig.7. 3D model of PCB1 with tetrahedral mesh and measured prototype: (a) Cap1 model; (b) Cap2 model; (c) Cap3 model; (d) measured prototype.

interaction between capacitor and PCB. Measurement and modeling results fits very well for all three proposed capacitor models. All three capacitor models provides almost identical impedance, therefore it can be concluded that their performance is equal in this current case.

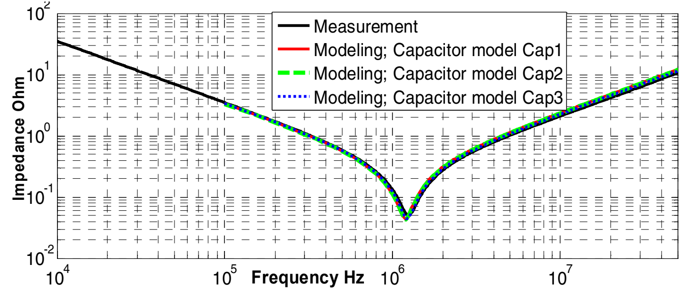

Fig.8. Impedance magnitude of PCB1 and capacitor.

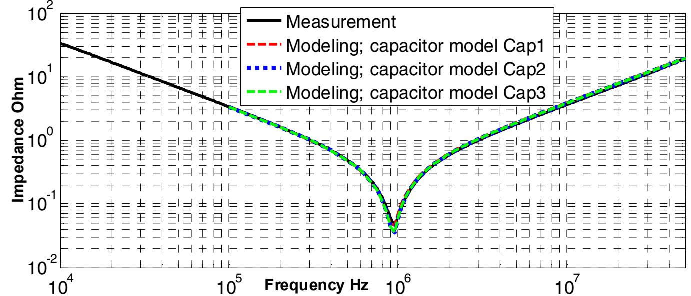

Fig.9. Impedance magnitude of PCB2 and capacitor.

B. Z_{11} parameter measurements if two capacitors are mounted on PCB

To verify the performance of both - PCB and all proposed capacitor models, measurements were carried out and input impedance at SMA port were measured. The 3D models for PCB1 with mounted capacitors, with tetrahedral mesh view and measured prototype are shown in Fig.10. In this case two capacitors are mounted in different distances from each other: 7mm, 17.5mm and 28mm, respectively. Distance between capacitors is measured between capacitor central axis. Therefore, impedance Z_{11} characterizes capacitors impedance, PCB layout impedance, interaction between capacitors and

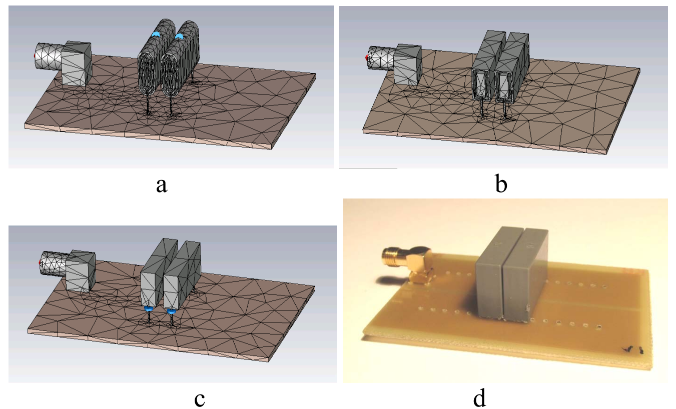

Fig.10. 3D model of PCB1 with tetrahedral mesh and measured prototype: (a) Cap1 model; (b) Cap2 model; (c) Cap3 model; (d) measured prototype.

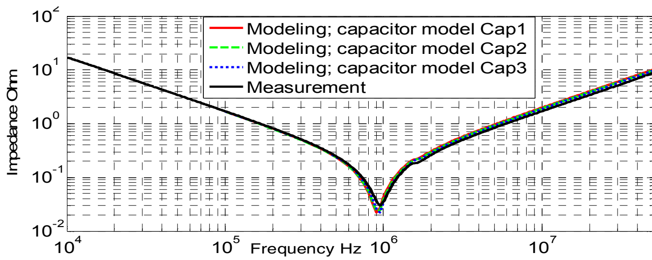

Fig.11. Impedance magnitude of PCB1 and capacitors in 28mm distance.

PCB and interaction between two capacitors - that is mutual inductance between capacitors, mainly. As an example the results were compared in Fig.11 for PCB1 and Fig.12 for PCB2, when the distance between the capacitors is 28mm. The

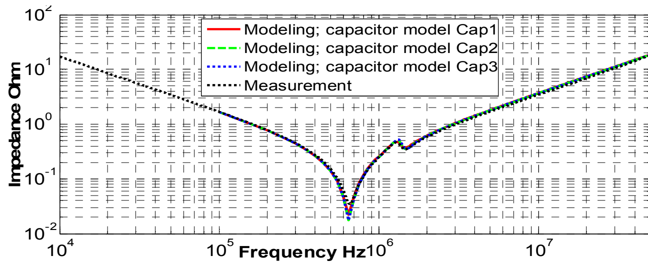

Fig.12. Impedance magnitude of PCB2 and capacitors in 28mm distance.

measurement and modeling results match very well for all PCB and capacitor models. The modeling precision can be evaluated in Fig.12, where resonance effect at 1.3MHz is modeled with high accuracy.

C. Two port S-parameter measurement if two capacitors are mounted on PCB

To verify the performance of both PCB and all proposed capacitor models, measurements were carried out and two port S-parameters at SMA ports were measured. PCB's in this case are slightly modified. One of the copper tracks has a 2mm split in the middle. Therefore, S_{21} and S_{12} parameters characterize the coupling of two loops, created by PCB and capacitors - mainly mutual coupling. The 3D model for PCB1 with mounted capacitor and measured prototype are shown in Fig.13. As an example the measurement and modeling results

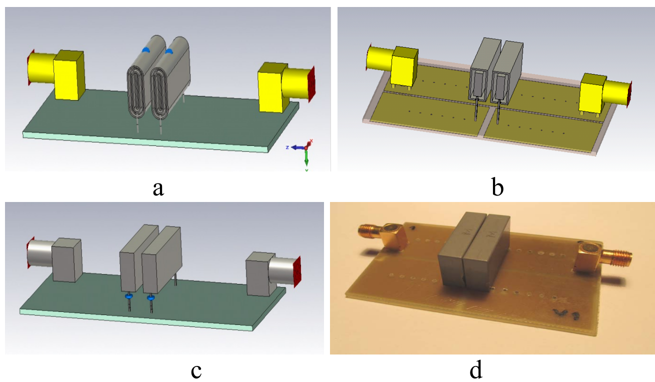

Fig.13. 3D model of PCB1 with a spitted track and measured prototype when capacitors are mounted in 7mm distance: (a) Cap1 model; (b) Cap2 model (transparency of PCB insulator changed to see the splited track); (c) Cap3 model; (d) measured prototype

for PCB1 are compared in Fig.14. It can be concluded that capacitor models Cap1, Cap2, Cap3 gives similar results and they are very close to modeling results for both PCB's.

V. CAPACITOR MUTUAL INDUCTANCE EXTRACTION

For mutual inductance M extraction from experimental and simulated results two extraction techniques can be used. The first technique proposed in [3] requires all the four S parameters as follows:

$$M = \frac{100 \cdot S_{21}}{2\pi f \cdot (1 - S_{22} + S_{22}S_{11} - S_{11} - S_{21}^2)}. \tag{1}$$

The second technique requires only $|S_{21}|$ to be measured or

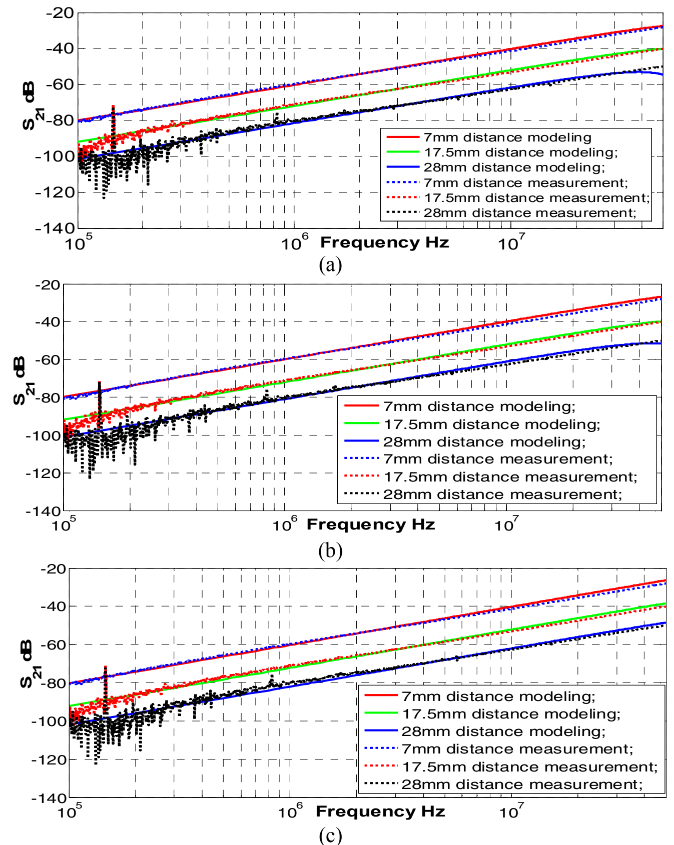

Fig.14. Transfer characteristics: (a) PCB1 with split track and capacitor model Cap1; (b) PCB1 with split track and model Cap2; (c) PCB1 with split track and model Cap3.

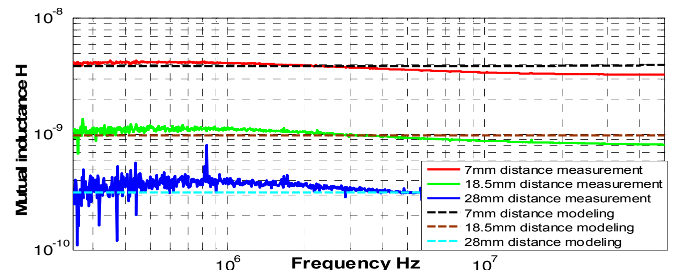

Fig.15. Extracted mutual inductance from measurements and modeled mutual inductance between capacitors on PCB1 with different distances for capacitor model Cap3.

simulated. Assuming that EMI filter capacitor impedance is much lower than 50Ω more simple expression for M extraction is derived in this paper:

$$M = 25\left|S_{21}\right|/(2\pi f) \quad . \tag{2}$$

Both expressions (1) and (2) give similar results. Taking a look on results in Fig.14 it can be concluded, that transfer parameter $|S_{21}|$ changes, if distance between capacitors is changed, therefore it can be concluded that mutual inductance between capacitors is changing. Comparing the $|S_{21}|$ for two PCB's, if the capacitors are in the same distance from each other, it can be concluded that PCB configuration has negligible effect on mutual inductance. As PCB configuration in this case has negligible effect on S_{21} parameter it, is obvious that it has negligible effect on mutual inductance, between two loops. Therefore, the mutual inductance between PCB tracks at both ports is ignored and for mutual inductance extraction between two capacitors Eqs. (1) or (2) can be used. As an example comparison of extracted mutual inductance results for PCB1 with Cap3 are presented in Fig.15. Measurement results in the lower frequency range is quite noisy, due to the low energy levels to be measured, measurement equipment noise floor and ambient noise (high peaks). Mutual inductance between two capacitors in distance 7mm at 1MHz is almost 4nH, in distance 18.5mm more than 1nH and distance almost 0.4nH. Mutual inductance has a slight drift over the frequency range; it can be explained by the measurement methodology and parasitic parameters not taken into account - such as connectors and theirs connection etc. and measurement error. All the capacitor models with PCB1 and PCB2 give equally similar results and are very close to extracted results from measurements.

M dependence on distance between capacitors is analyzed using Cap3 capacitor models and PCB2 model in CST MSW modeling environment. It can be done also with other capacitor models and PCB1. The results are presented in Fig.16. M decreases if distance between capacitors is increased.

VI. Mutual Inductance Reduction Techniques

Mutual inductance between capacitors is mainly created by the capacitor loops. One of the solutions is to reduce the capacitor created loop area. Mounting the capacitor as close to the PCB as possible gives positive result, but there still is loop created by internal construction. This could be changed, if component manufacturers modified the component internal structure. But also this step has its limitations, due to insulation thickness between internal conductive parts and surrounding environment. Therefore, external add-ons can, such as, ground plane on PCB and shielding, can be employed to reduce mutual coupling between capacitors. There is proposed shielding configuration between capacitors to reduce mutual coupling in Fig.17(a). The shielding performance is evaluated by measuring S_{21} and by modeling in CST MSW. For modeling capacitor models Cap3 have been used. The model is shown in Fig.17(b). On top of PCB copper solid ground plane (GND) is added. Afterwards, copper shielding is added between capacitors. The connection and configuration of ground plane and shielding is extremely important. There have been made measurements and modeling for various configurations. Measurement results are shown in Fig.18. Modeling results are compared with measurement results in Fig.19. For modeling all conductive parts are modeled as perfect electric conductor, to reduce calculation time and memory usage.

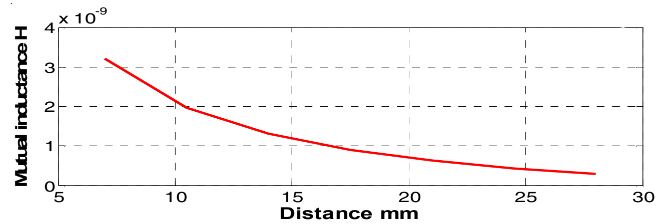

Fig.16. Extracted mutual inductance versus distance between capacitors.

At first, PCB is measured without ground plane and shielding to have a reference. Then ground plane is added. During the measurement the ground plane is floating. In Fig.18 it is clear, that ground plane increases coupling between two capacitors as transfer coefficient S_{21} increases by few dB. Then copper shielding is added between two capacitors, without soldering it to ground plane. It should be noted, that shielding material touches the ground plane of PCB, but due to imperfections, it is not solid contact in full length. In Fig.18, it is visible, that coupling is reduced as S_{21} is reduced by 8dB. Further, shielding is soldered to ground plane at two and later at three points, as it is usually done in PCB fabrication, when thru hole mounting of shielding is used. Transfer coefficient decreases by 15dB to 17dB, thus reducing mutual inductance between capacitors. Finally, shielding is soldered along whole length to the PCB ground plane. Transfer coefficient reduces by more than 30dB. At frequencies up to 1MHz, transfer coefficient S_{21} is so low, that in Fig.18 VNA noise is measured. The difference, when the shielding is connected in three or two points to ground plane and when the shielding is connected in whole length is huge, if transfer coefficient is measured. Therefore, with the help of surface current modeling in CST MSW the difference between two situations can be explained. If copper shield between capacitors is not connected in whole length eddy currents are induced on both sides of shield due to the gaps in shielding, where the current can penetrate. If the copper shielding is soldered in whole length the eddy currents have no gap to penetrate between two copper conductors.

To directly analyze shielding configuration impact on mutual inductance between two capacitors, mutual inductance has been extracted from measurement results. Shielding with continuous connection to ground plane has the best result, 12pH mutual coupling between capacitors at 1MHz. If shielding is connected at two or three points only mutual

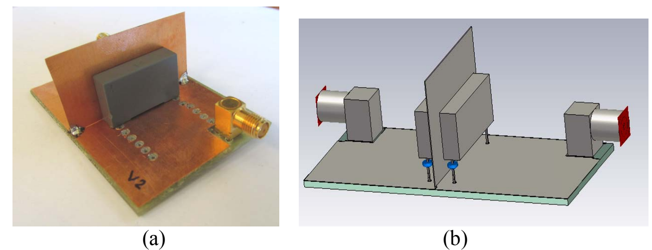

Fig.17. (a) Shielding configuration to reduce mutual coupling between capacitors with two connection points (soldered) between GND plane and copper shield; (b) model for shielding evaluation between capacitors using Cap3 capacitor models.

inductance increases up to 78pH and 61pH at 1MHz, respectively. If copper shielding is not connected at all but only placed between two capacitors the mutual inductance reaches 1.7nH at 1MHz. If no shielding and ground plane are used the coupling is 3.7nH.

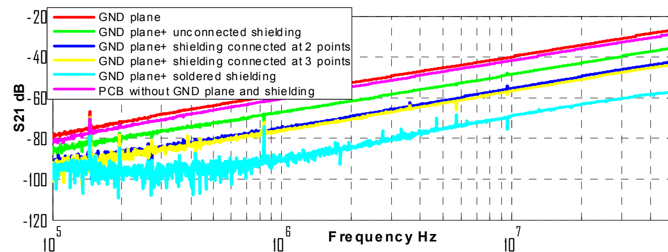

Fig.18. Measurement results of various shielding techniques to reduce mutual coupling between capacitors.

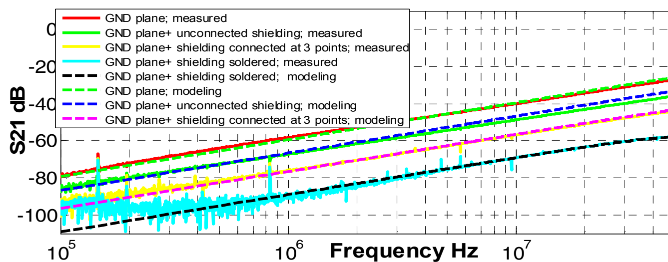

Fig.19. Measurement and modeling results comparison of various shielding techniques to reduce mutual coupling between capacitors.

CONCLUSION

Capacitors can be modeled using 3D electromagnetic software tools available in the market. In this paper modeling has been done using CST MWS. Three capacitor models have been proposed - Cap1, Cap2, Cap3. All proposed models during the verification have shown that their performance is high enough to enable PCB mounted capacitor modeling and mutual inductance modeling between capacitors. Difference between the proposed capacitor models lays in their complexity, that has direct impact on computational time and occupied memory. The first model - Cap1, have the most complex structure having curved faces and round connectors. Therefore, it in great details represents the real capacitor without outer insulation shell. Capacitor models Cap2 and Cap3 are created using rectangular shapes only that leads to lower mesh requirements and lower memory consumption, accordingly. Capacitor model - Cap3 have the lowest meshcell number and the lowest modeling time whatever solver is used and whatever mesh type is used. In all verification steps all capacitor models have shown that it is possible to model capacitors and their couplings to PCB and other capacitors with great accuracy. Therefore, all capacitor models can be used for this purpose. Therefore capacitor model- Cap3 has at least 20% lower meshcell number in case if hexahedral mesh type is chosen, compared to capacitor model - Cap2 and at least 150% lower meshcell number compared to capacitor model Cap1. Capacitor model - Cap3 has at least 49% lower meshcell number in case if tetrahedral mesh type is chosen, compared to capacitor model - Cap2 and at least 400% lower meshcell number compared to capacitor model Cap1. Using both solvers and different mesh types it is obvious that Cap3 model calculation takes at least 30% less than Cap2 calculation and at least 250% less time than Cap1 calculation, if frequency domain solver with hexahedral mesh is used. For time domain solver the difference in calculation time is higher - Cap3 model calculation takes at least 16% less than Cap2 calculation and at least 1280% less time than Cap1 model calculation. Capacitor model Cap3 is recommended to use in further EMI filter modeling.

Mutual inductance reduction techniques have been proposed, measured and modeled. Modeling results follow the measurement results very well and again proves that 3D electromagnetic field modeling can be successfully used in RFI filter modeling. Proposed shielding technique when copper shielding is soldered to ground plane in whole length, reduces mutual coupling between capacitors from 3.7nH to 12pH at 1MHz. Other shielding techniques also reduces mutual coupling, but the results are not so good. In case, if only ground plane is added on top of PCB to reduce mutual coupling between capacitors, the opposite result is achieved- mutual coupling is increased.

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