Evaluation of Quasi-resonant DC Link Topologies for Soft Switching of Multiple DC-inputs Three Phase Inverter

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Abstract

Possible soft-switching solutions for a Multiple DC-inputs Direct Electric Power Converter are investigated. Quasi-Resonant DC link circuits are considered for the task. By optimizing the resulting combination, a novel topology is developed. The resonant operation in combination with multiple power sources is modelled. Equations for the resonant circuit trip current calculation are adjusted to support dual input operation.

Introduction

Modern electric propulsion systems often comprise a couple of different energy sources [1]. For example, the electrical machine of a hybrid-electrical passenger automobile may draw power from an internal combustion engine driven electrical generator or a hydrogen fuel cell while using a battery pack or a boost capacitor for accumulation of regenerated or previously stored electrical energy [2]. In case of a public transportation vehicle, e.g. a trolleybus, the primary energy source - a connection to an electrical grid - can be supplemented by a boost capacitor for regenerative braking [3]. Besides propulsions systems, renewable energy generation, e.g. in households, also requires solutions for connecting different DC voltages to a single AC grid [4].

Different strategies exist for connecting multiple DC power sources to an inverter and ensuring proper power flow. In the most basic case, sources can be coupled to the main DC bus by DC-DC converters as in Fig. 1 [5]. This can turn out suboptimal in terms of system volume and efficiency.

However, topologies exist for connecting both DC inputs directly to a motor inverter to avoid the additional volume and losses of a DC-DC converter. For example, two regular three-phase inverters can

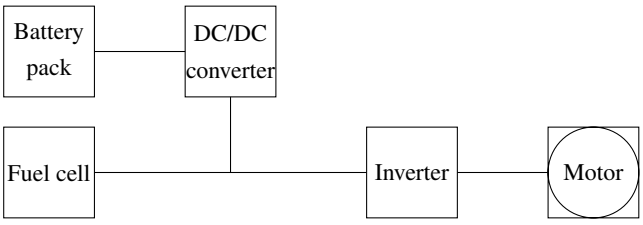


Fig. 1: A standard architecture example for multiple DC power source connection to the motor

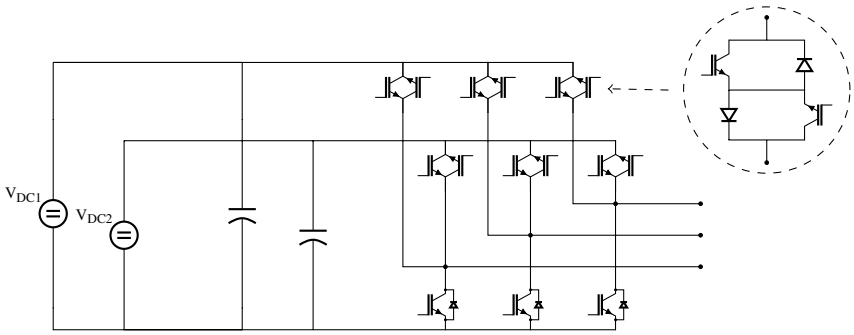


Fig. 2: Circuit topology of a hard switched multiple DC inputs inverter as described in [5]

be connected each to their own DC power source with the open-winding machine phases connected in series between them [6]. Despite several benefits, this setup requires a six-wire cable and increases the conduction losses when only one DC power source is utilized.

Reference [5] investigates an inverter topology with two input DC links - the multiple DC-inputs Direct Electric-Power Converter (D-EPC). As seen in Fig. 2, both DC links share the lower inverter legs, but the positive DC link rails are connected separately by bidirectional switches to avoid short circuiting.

The control of D-EPC differs only slightly from casual vector control systems. The output AC power is divided between the DC input sources according to system status. The power distribution coefficient of a given DC source can also be negative in case of charging. A time allotment (time-share) strategy is then implemented as the PWM pulses are alternately drawn from each DC source [5].

One of the main drawbacks of this topology is the large number of bidirectional switches that eventually requires even more transistors than the aforementioned two-inverter scheme and increases the conduction losses. However, the integration and efficiency of bidirectional switches is subject to progress [7], [8] increasing the future potential of such topologies.

Switching losses constitute a notable portion of the overall losses in modern hard-switched converters due to increasing switching frequencies that aim to reduce the size of passive components. This paper entertains the possibility to eliminate switching losses from the D-EPC by adding soft-switching capabilities.

From several resonant topologies that enable soft switching the Quasi-Resonant DC Link principle is chosen for integration with the D-EPC. Therefrom a novel Dual Input Quasi-Resonant DC Link Inverter (DIQRDCLI) topology is proposed by disposing of redundant switches in the combination.

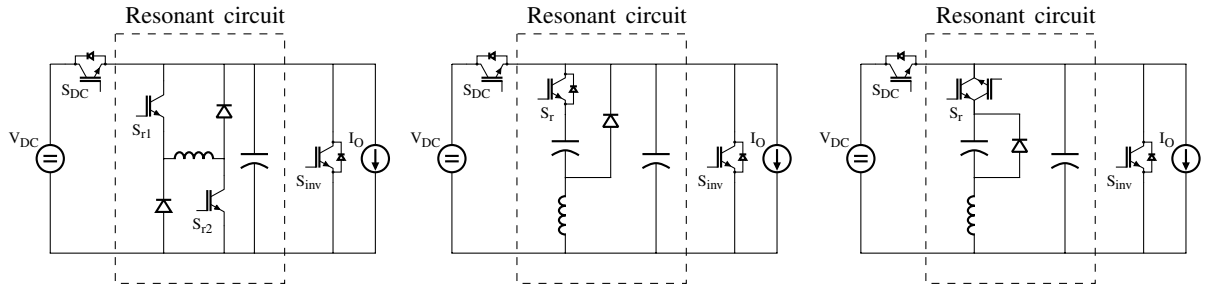
Soft switching for variable frequency drives

A common approach for achieving soft switching is the use of various resonant circuits that utilize the resonant properties of LC circuits to provide ZVS or ZCS periods for the commutation of power switches.

Numerous principally different types of resonant circuits exist, most of which are only capable of providing fixed-shape output voltage pulses, the shape of which may also depend on the load current [9]. In case of fixed shape output pulses, voltage is modulated by discrete pulse modulation [10], [11] or pulse density modulation [12] that yields undesirable harmonic components (of the resonant frequency) in the output voltage [13], [14].

In AC-AC applications, high performance space vector modulation (SVM) can be achieved by using a Partial Resonant Link AC-AC Converter that demonstrates a quite unique modulation strategy [15].

However, for high performance in a DC-AC system, use of PWM should be enabled, thus output voltage pulses must be of variable duration. This is achieved by the Quasi-Resonant DC Link Inverter (QRDCLI) family. Here, as the name suggests, the resonant process takes place only a fraction of the time. No energy is stored in the resonant circuit during the PWM on-state and the resonance is manually initiated only in time for each commutation [16].



(a) Three switch topology (b) Reduced resonant current topology (c) Lossless zero-voltage interval topology

Fig. 3: Various circuit topologies of a Quasi-Resonant DC Link Inverter as described in [17]

A variety of different QRDCLI topologies has been presented in the last several decades. Detailed working principles, waveforms and modulation strategies of some can be found in [13], [17], [18], [19], [20], [21] and [22] for example.

Fig. 3 shows three examples of a QRDCLI investigated in [17]. The switch S_{inv} together with the current source I_O represent an equivalent circuit of a three phase inverter bridge connected to an inductive load. The current is assumed constant during a single switching cycle.

In these topologies the LC components are utilized differently, but the main operational sequence to achieve soft switching remains the following:

1. the resonant circuit is pre-charged until a specified trip current in the inductor is reached,
2. the DC link switch S_{DC} is opened under ZVS condition,
3. the inductor current together with the load current proceed to discharge the DC link capacitor thereby pulling the DC link voltage down to zero,
4. the zero DC link voltage is maintained until the required inverter commutation is complete,
5. the energy stored in the resonant circuit is utilized to recharge the DC link capacitor up to the supply voltage,
6. S_{DC} is closed under ZVS condition, thus reconnecting the DC supply to the load.

Aside from the switching loss elimination, gradual DC link capacitor charging (steps 3. and 5.) decreases the voltage gradients of PWM pulse edges (see Fig. 6). Limiting *dv/dt* decreases output noise and overvoltages caused by wave reflection in cables. This can reduce the output filter requirements an enhance system dynamics [17]. Also, an additional switch may be utilized to disconnect the negative DC supply rail as well. This way common mode voltages can be greatly reduced [17].

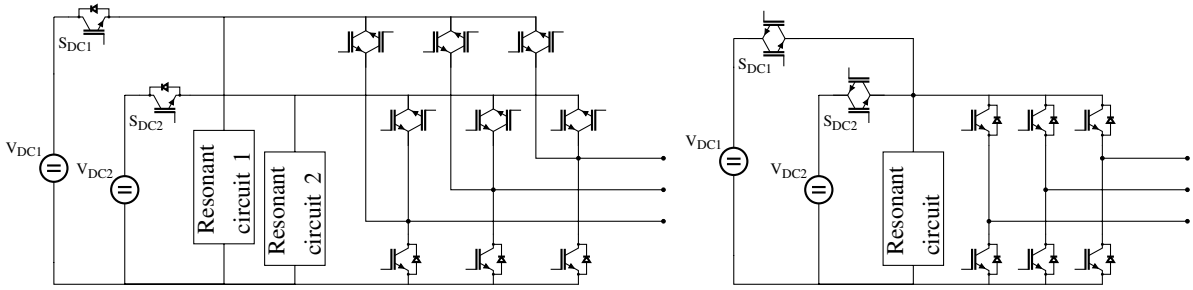
Another important feature of the QRDCLI circuits is the variable zero voltage interval (see step 4.). During this time, the energy is stored inside the resonant inductor (Fig. 3a), the resonant capacitor (Fig. 3c) or both (Fig. 3b). The extended zero voltage interval can be utilized as zero vector V_{07} in modified space vector PWM [16].

Besides the properties mentioned above, most attention of this paper is directed to the ability of the QRDCLI to raise the DC link voltage to an arbitrary value, depending on the amount of stored energy. This feature makes it suitable for integration with the D-EPC topology as further described.

Proposed optimization

Fig. 4a shows a straightforward way to implement the QRDCL on a D-EPC topology. Each inverter input rail has a supply disconnection switch and a separate resonant circuit (R.C.) connected to the negative rail. The ”black boxes” *Resonant curicuit 1* and *Resonant circuit 2* represent the possibility to utilize any one of the three resonant circuits shown in Fig. 3 (or any other parallel QRDCL circuit).

As described in the next chapter, R.C. will raise the voltage of the connected DC link to an arbitrary value. Therefore, given that sufficient energy is stored in the R.C., it can be charged from one DC link



(a) Multiple DC inputs Inverter combined with separate QRDCL's (b) Proposed novel DIQRDCLI general topology with reduced part count

Fig. 4: Possible implementation of QRDCL in a dual input inverter

and subsequently used to charge the other DC link (having a different voltage). This way a single R.C. could theoretically be used by alternately connecting it to each of the two DC link positive rails.

However, if only a single R.C. would be used, it can be seen that because of supply disconnection switches S_{DC1} and S_{DC2} one of the D-EPC inverter bridge's upper sections becomes redundant. As the positive rails are only alternately connected to their respective power sources, they can be merged together, thus returning to a classic six switch three phase inverter bridge. The resulting topology, a DIQRDCLI (Dual Input QRDCLI), is shown in Fig. 4b.

Immediately, though, it can be seen that the supply disconnection switches need to be bidirectional ones to avoid short circuiting of the power sources through the body-diode. The resulting load current path eventually inherits an additional switch from both the D-EPC and QRDCLI making the load current pass through four switches in series as opposed to two switches for a hard switched single input inverter bridge.

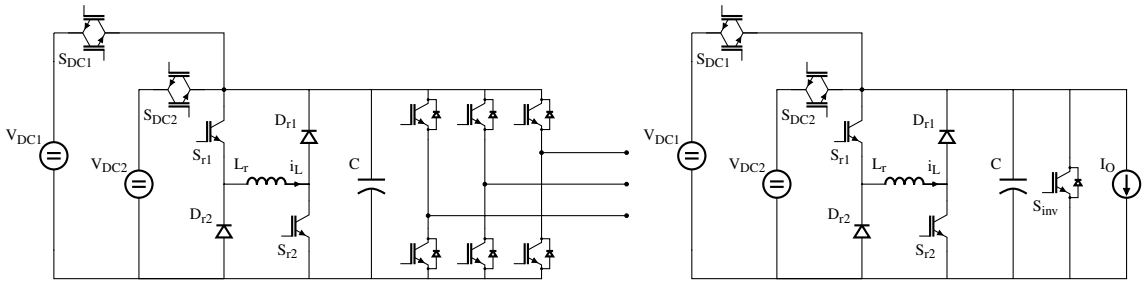
Even so, when comparing to the D-EPC in Fig. 2, DIQRDCLI gains the following:

- the switch count has been reduced from 15 to 11 or 12 (depending on the R.C. selection),
- soft switching of every switch is obtained, reducing switching losses,
- voltage gradient values *dv/dt* can now be reduced.

Three switch topology example - detailed operation

The simplest quasi-resonant DC link in terms of operation principle is the three switch topology that was first introduced in 1991 [13]. Here the three switch topology is chosen to exemplify the operation of DIQRDCLI (Fig. 5).

Efficient operation of the resonant circuit relies on optimized selection of the trip current I_I. This is the resonant inductor current value at which the voltage source is disconnected. The magnetic energy stored in L_r must suffice to discharge and recharge capacitor C while also temporarily providing the output current I_O.



(a) Full topology (b) Simplified circuit

Fig. 5: A DIQRDCLI example topology using the three switch quasi-resonant DC Link from [13]

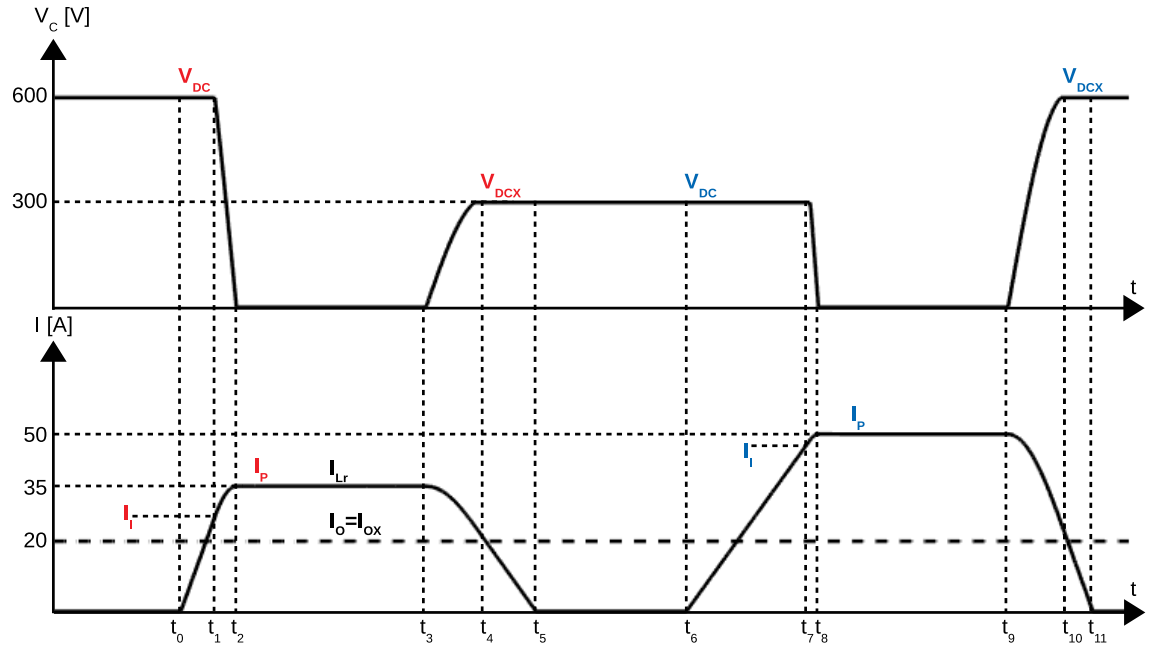


Fig. 6: Simulated waveforms of a single operational cycle
$V_{DC1} = 600V$, $V_{DC2} = 300V$, $I_O = I_{OX} = 20A$, $L_r = 60\mu H$ and $C = 150nF$
Parameters in red refer to the first resonant cycle while those in blue refer to the second resonant cycle

The trip currents are calculated by separately analysing the operational modes and the required border states between modes that enable soft switching of the power devices. The equivalent circuits of each mode are shown in Fig. 7. Simulated waveforms with indicated border values are presented in Fig. 6.

The differential equations for the equivalent circuits have been solved in [13] and further analysed in [17], but the resulting state equations shall be revised here for the dual input case as well as to clarify the operational principle.

The existing expressions needed to be slightly updated to take into consideration different input voltages before and after the resonant cycle. Distinction between V_{DC} and V_{DCX} was made. V_{DC} is assumed to be the voltage from which the resonant circuit is charged and V_{DCX} - the voltage to which the capacitor C needs to be recharged before re-coupling to the corresponding power source. For example, if $V_{DC} = V_{DC1}$ and $V_{DCX} = V_{DC2}$ during a given resonant cycle, then during the next one: $V_{DC} = V_{DC2}$ and $V_{DCX} = V_{DC1}$.

It should be noted that it actually takes 12 separate modes for the whole operational cycle to complete and return to the initial state. However, the operational cycle consists of two resonant cycles, therefore modes 6 through 11 are symmetric to modes 0 through 5. The same equations are used in both resonant cycles. In both cases the first voltage is denoted by V_{DC} and the second one by V_{DCX}.

Mode 0 ($...t_0$)

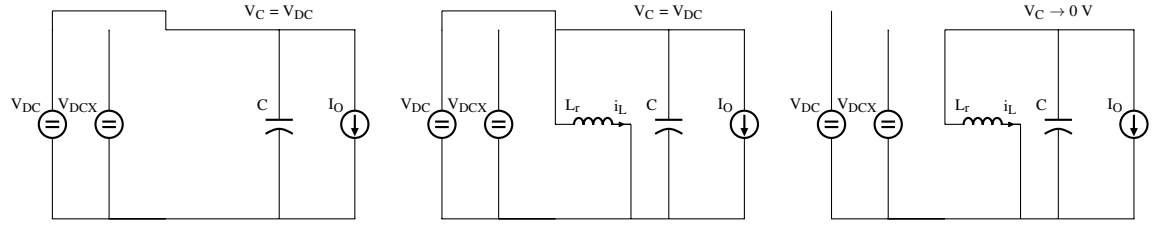
Output current is fully supplied by V_{DC} (In this case V_{DC1}) for a desired time period. The resonant inductor L_r is disconnected and stores no energy while the resonant capacitor C is under input voltage:

$$i_{Lr}(t) = 0 \quad \text{and} \quad v_C(t) = V_{DC} = V_{DC1}. \tag{1}$$

Mode 1 ($t_0...t_1$)

The resonant inductor is connected through switches S_{r1} and S_{r2} at time instant t_0. The switching happens under zero current conditions because of the series inductor. Inductor current rises linearly to a selected value I_I, which is the trip current. Capacitor voltage remains unchanged.

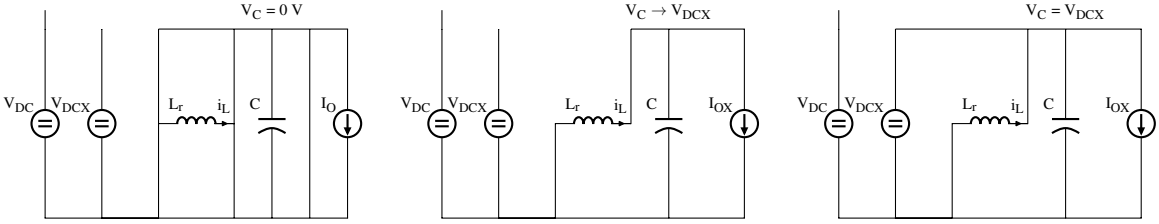
$$i_{Lr}(t) = \frac{V_{DC}}{L_r}(t - t_0) \quad \text{and} \quad v_C(t) = V_{DC} = V_{DC1}. \tag{2}$$



(a) Mode 0: the resonant inductor is not connected and V_{DC} is connected to the inverter bridge

(b) Mode 1: resonant inductor is connected to V_{DC} and charged up to I_I

(c) Mode 2: supply voltage V_{DC} is disconnected and the resonant capacitor C is discharged



(d) Mode 3: zero voltage period with freewheeling currents; the inverter bridge commutation takes place

(e) Mode 4: resonant switches are turned off and the resonant capacitor C is charged to voltage V_{DCX}

(f) Mode 5: the DC link is connected to V_{DCX} and residual inductor current I_R returned to the system

Fig. 7: Operation modes of a DIQRDCLI during a single resonant cycle; here $V_{DC1} = V_{DC}$ and $V_{DC2} = V_{DCX}$

Mode 2 ($t_1 \ldots t_2$)

At time instant t_1 the switch S_{DC1} is opened under zero voltage conditions. In the following resonant process the capacitor is discharged by the inductor current with an offset of I_O. By solving the differential equations of the circuit in Fig. 7c, expressions (3) and (4) are obtained.

A resonant impedance $Z_r = \sqrt{L_r/C}$ is defined.

$$i_{Lr}(t) = \frac{V_{DC}}{Z_r} sin(\omega_r(t-t_1)) + (I_I + I_O)cos(\omega_r(t-t_1)) - I_O, \tag{3}$$

$$v_C(t) = V_{DC} cos(\omega_r(t-t_1)) - Z_r(I_I + I_O)sin(\omega_r(t-t_1)). \tag{4}$$

At the end of mode 2 (t_2) when the capacitor is completely discharged, inductor current has reached its peak value I_P. Knowing that $v_C(t_2) = 0V$, the value of I_P can be expressed from (3) and (4):

$$I_P = i_{Lr}(t_2) = \sqrt{(I_I + I_O)^2 + \left(\frac{V_{DC}}{Z_r}\right)^2} - I_O, \tag{5}$$

Mode 3 ($t_2 \ldots t_3$)

As the capacitor voltage drops to zero, the inductor current proceeds to freewheel through resonant diodes D_{r1} and D_{r2}. All the upper or lower inverter bridge switches are turned on providing a freewheeling path for the load current. Thus the equivalent inverter switch S_{inv} in Fig. 5b.

The capacitor voltage remains at 0V during mode 3 and (if conduction loss is disregarded) the inductor current maintains its peak value:

$$v_C(t) = 0V \quad \text{and} \quad i_{Lr}(t) = I_P. \tag{6}$$

At the end of mode 3 (t_3) the next inverter bridge state is engaged with ZVS and the output current changes it's value to I_{OX} which is defined by the switch states.

Mode 4 ($t_3 \ldots t_4$)

At t_3 switches S_{r1} and S_{r2} are opened under zero voltage conditions and capacitor C is now recharged by the resonant inductor current with an offset current of I_{OX}. Solving the differential equations of the circuit in Fig. 7e gives the expressions:

$$i_{Lr}(t) = (I_P - I_{OX})cos(\omega_r(t - t_3)) + I_{OX}, \tag{7}$$

$$v_C(t) = Z_r(I_P - I_{OX})sin(\omega_r(t - t_3)). \tag{8}$$

Unlike with a single input QRDCLI the capacitor is now charged up to V_{DCX} during mode 4. Thereby $V_C(t_4) = V_{DCX} = V_{DC2}$. By applying this to equations (7) and (8) the residual inductor current at the end of mode 4 can be expressed as:

$$i_L(t_4) = I_R = \sqrt{(I_P - I_{OX})^2 - \left(\frac{V_{DCX}}{Z_r}\right)^2} + I_{OX}. \tag{9}$$

At t_4 switch S_{DC2} is closed under zero voltage conditions and the load is directly connected to V_{DCX}.

Mode 5 ($t_4 \ldots t_5$)

After connecting the power supply inductor current value falls linearly from I_R to zero as energy is returned to the system:

$$i_{Lr}(t) = I_{OX} - \frac{V_{DCX}}{L_r}(t - t_4) \quad \text{and} \quad v_C(t) = V_{DCX}. \tag{10}$$

Trip current calculation

Calculation of optimal trip currents for the three switch QRDCLI topology is described in [17], where the expressions are derived for four cases (I-IV) depending on the direction (positive or negative) of the output current before the inverter bridge commutation (I_O) and after it (I_{OX}).

As mentioned before, for the case of dual input operation both V_{DC} and V_{DCX} need to be taken into account. Also, considering the extra layer of the trip current table introduced by V_{DCX}, the expressions will be generalized to fit all of the I_O & I_{OX} combinations simultaneously.

First, the minimum value of I_R is defined by I_{OX}. If I_{OX} is positive, inductor should be able to provide all of it at t_4 or else the capacitor will start discharging before reaching V_{DCX}. Also, when possible, matching the inductor current with the output current at the moment of power source commutation (both t_1 and t_4) provides both ZCS and ZVS for the source coupling switches. If I_{OX} is negative it adds to the charging of C and it is *assumed* that the required $I_{Rmin} = 0A$ [17]:

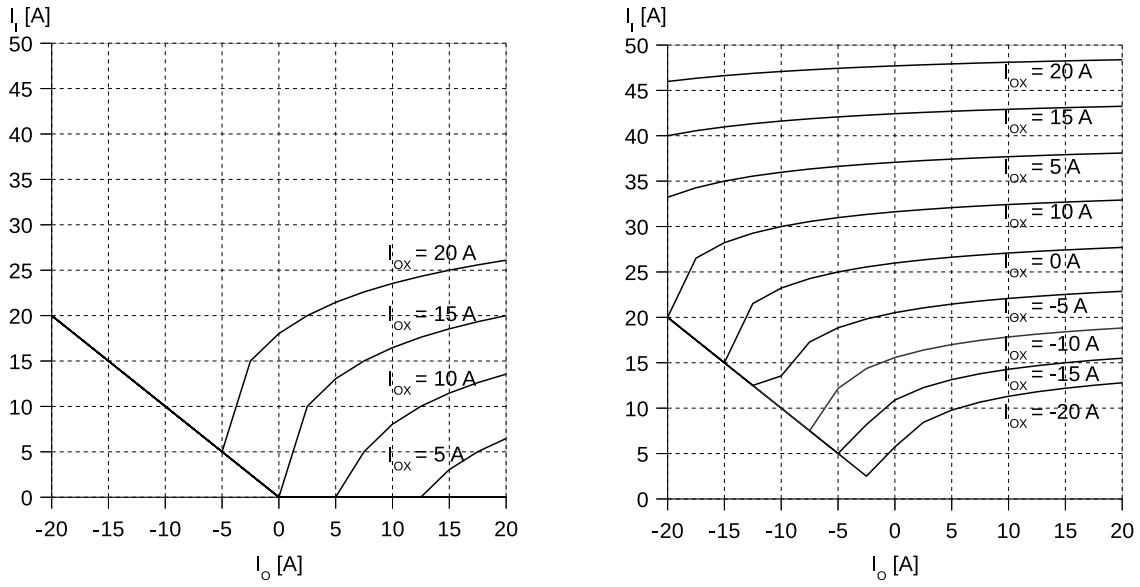
$$I_{Rmin} = max[I_{OX}, 0]. \tag{11}$$

The minimum peak inductor current I_{Pmin1} that can provide this minimum residual current I_{Rmin} is expressed from (9) as:

$$I_{Pmin1} = \sqrt{(I_{OX} - I_{Rmin})^2 + \left(\frac{V_{DCX}}{Z_r}\right)^2} + I_{OX}. \tag{12}$$

Another minimum constraint for the inductor current peak value is defined in [17] as:

$$I_{Pmin2} = \frac{V_{DC}}{Z_r} - I_O. \tag{13}$$



(a) $V_{DC} = 600V$ and $V_{DCX} = 300V$

(b) $V_{DC} = 300V$ and $V_{DCX} = 600V$

Fig. 8: Calculated trip currents for a converter with input voltages $V_{DC1} = 600V$ and $V_{DC2} = 300V$ and resonant components $L_r = 60\mu H$ and $C = 150nF$

It can be seen that placing this value in (15) results in a minimum trip current of $I_{Imin2} = -I_O$. This is because with a negative output current I_O, the inductor current needs to provide all of it at t_1 or else the output current will put additional charge on the capacitor creating a voltage spike.

A minimum peak value that can satisfy both constraints is chosen:

$$I_{Pmin} = max[I_{Pmin1}, I_{Pmin2}]. \tag{14}$$

Next, minimum trip current I_{Imin} that can provide the required inductor peak current I_{Pmin} is expressed from (5) as:

$$I_{Imin} = \sqrt{(I_{Pmin} + I_O)^2 - \left(\frac{V_{DC}}{Z_r}\right)^2} - I_O. \tag{15}$$

Using the five steps (11) to (15) trip currents were calculated for a system with supply voltages $V_{DC1} = 600V$ and $V_{DC2} = 300V$. Adequate LC values were referred from [17] as $L_r = 60\mu H$ and $C = 150nF$. The calculated trip current values are shown in Fig. 8.

Further possibilities for decreasing inductor loss

It should be noted that when the calculated minimum trip current (15) is negative, a practical minimum of $I_{Imin} = 0A$ is assumed. However, even when the calculated minimum trip current is positive, this value is not always necessary to provide soft switching conditions for the converter.

This is because when $I_{OX} < 0$ it is assumed that $I_{Rmin} = 0A$, i.e. that inductor current I_{Lr} falls to zero no sooner than t_4 so that it can fully charge the capacitor up to V_{DCX}. However, in case I_{Lr} drops to 0 before t_4, a negative output current will fully recharge the capacitor (if the value of $|I_{OX}|$ is sufficient). Considering this the actual trip current could be decreased until one of the other constraints is met. These constraints are I_{Pmin2} and the acceptable duration of $(t_4 - t_3)$.

As mentioned before, the constraint of I_{Pmin2} is set to prevent a voltage spike at t_1 in case of $I_O < 0$. By inserting (13) into (15) it can be seen that a positive output current $I_O > 0$ yields zero minimum trip

current $I_{Imin} = 0$.

These two circumstances allow to conclude that if $I_O > 0$ and $I_{OX} < 0$, the soft switching conditions can be produced without engaging the resonant inductor L_r at all as the capacitor C will be discharged by I_O and recharged by I_{OX}.

Choosing this strategy, the duration of $(t_2 - t_1)$ and $(t_4 - t_3)$ would rapidly increase with decreasing output current values therefore decreasing the operational range of space vector PWM. Nevertheless, considering that theoretically almost a quarter of inductor cycles can be cancelled and an additional fraction of resonant cycles can be performed with decreased trip currents, the customization of the control strategy shows potential for loss reduction in the resonant inductor circuit.

Conclusion

Thanks to completely parallel topologies, full PWM ability and other beneficial features the quasi-resonant DC link principle is suggested for optimizing the topology and operation of a D-EPC converter. With the introduced DIQRDCLI topology group, device count is reduced while adding soft switching for all devices and output voltage gradient control.

Equations for trip current calculation have been adjusted to suit the dual input operation. The equations have also been generalized to suit all output current direction combinations.

Analysing the trip current equations reveals potential for further improvement of resonant circuit efficiency through a more complicated control algorithm.

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